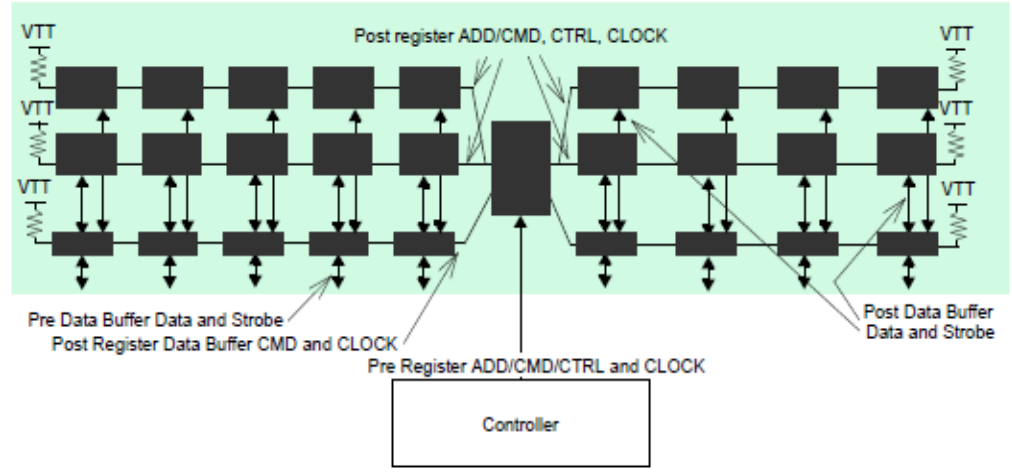
Exhibit 5

US Patent No. 7,619,912

Exhibit 5

’912 Patent	Accused Instrumentalities
CLAIM 16	
[16pre] A memory module connectable to a computer system, the memory module comprising:	Samsung and Google have claimed that Samsung sells in the US to Google DDR4 LRDIMM and RDIMM that employ PDA (the “Disputed Memory Modules”). The JEDEC Standard No. 21C specification “follows the JEDEC standard DDR4 component specification JESD79-4.” JEDEC Standard No. 21C (Aug. 2015), at Page 4.20.27-5. In Figure 3, reproduced below, the JEDEC Standard No. 21C specification provides an example of LRDIMM topologies illustrating the connection between the memory module and the memory controller of a computer system.  **Figure 3 — LRDIMM Topologies** JEDEC Standard No. 21C (Aug. 2015), at Page 4.20.27-17.

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'912 Patent	Accused Instrumentalities
	In accordance with the JEDEC Standard No. 21C specification, the DDR4 LRDIMM socket pin wiring assignment for connecting to a memory controller of a computer system is provided in Table 5, reproduced below.

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Table 5 — DDR4 288 Pin LRDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label
12 V, NC	1	145	*12 V,* NC
VSS	2	146	VREFCA
DQ4	3	147	VSS
VSS	4	148	DQ5
DQ0	5	149	VSS
VSS	6	150	DQ1
DQS9_t, *DM0_n, DBI0_n, NC*	7	151	VSS
TDQS9_c, DQS9_c, *NC*	8	152	DQS0_c
VSS	9	153	DQS0_t
DQ6	10	154	VSS
VSS	11	155	DQ7
DQ2	12	156	VSS
VSS	13	157	DQ3
DQ12	14	158	VSS
VSS	15	159	DQ13
DQ8	16	160	VSS
VSS	17	161	DQ9
_t, DQS10_t, *DM1_n, DBI1_n, NC*	18	162	VSS
TDQS10_c, DQS10_c, *NC*	19	163	DQS1_c
VSS	20	164	DQS1_t
DQ14	21	165	VSS
VSS	22	166	DQ15
DQ10	23	167	VSS
VSS	24	168	DQ11
DQ20	25	169	VSS
VSS	26	170	DQ21
DQ16	27	171	VSS
VSS	28	172	DQ17
_t, DQS11_t, *DM2_n, DBI2_n, NC*	29	173	VSS
TDQS11_c, DQS11_c, *NC*	30	174	DQS2_c
VSS	31	175	DQS2_t
DQ22	32	176	VSS
VSS	33	177	DQ23
DQ18	34	178	VSS
VSS	35	179	DQ19
DQ28	36	180	VSS
VSS	37	181	DQ29
DQ24	38	182	VSS
VSS	39	183	DQ25
_t, DQS12_t, *DM3_n, DBI3_n*	40	184	VSS

Front Side Pin Label	Pin	Pin	Back side Pin Label
CK0_t	74	218	CK1_t
CK0_c	75	219	CK1_c
VDD	76	220	VDD
VTT	77	221	VTT
	KEY		
EVENT_n	78	222	PARITY
A0	79	223	VDD
VDD	80	224	BA1
BA0	81	225	A10/AP
RAS_n/A16	82	226	VDD
VDD	83	227	RFU
CS0_n	84	228	WE_n/A14
VDD	85	229	VDD
CAS_n/A15	86	230	NC, *SAVE_n*
ODT0	87	231	VDD
VDD	88	232	A13
CS1_n, *NC*	89	233	VDD
VDD	90	234	*NC,* A17
ODT1	91	235	*NC,* C2
VDD	92	236	VDD
C0, CS2_n, *NC*	93	237	*NC,* CS3_n, C1
VSS	94	238	SA2
DQ36	95	239	VSS
VSS	96	240	DQ37
DQ32	97	241	VSS
VSS	98	242	DQ33
TDQS13_t, DQS13_t, *DM4_n, DBI4_n, NC*	99	243	VSS
TDQS13_c, DQS13_c, *NC*	100	244	DQS4_c
VSS	101	245	DQS4_t
DQ38	102	246	VSS
VSS	103	247	DQ39
DQ34	104	248	VSS
VSS	105	249	DQ35
DQ44	106	250	VSS
VSS	107	251	DQ45
DQ40	108	252	VSS
VSS	109	253	DQ41
TDQS14_t, DQS14_t, *DM5_n, DBI5_n, NC*	110	254	VSS
TDQS14_c, DQS14_c, *NC*	111	255	DQS5_c

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Table 5 — DDR4 288 Pin LRDIMM Pin Wiring Assignments (Cont'd)

Front Side Pin Label	Pin	Pin	Back side Pin Label
TDQS12_c, DQS12_c, *NC*	41	185	DQS3_c
VSS	42	186	DQS3_t
DQ30	43	187	VSS
VSS	44	188	DQ31
DQ26	45	189	VSS
VSS	46	190	DQ27
CB4, *NC*	47	191	VSS
VSS	48	192	CB5, *NC*
CB0, *NC*	49	193	VSS
VSS	50	194	CB1, *NC*
_t, DQS17_t, *DM8_n, DBI8_n, NC*	51	195	VSS
TDQS17_c, DQS17_c, *NC*	52	196	DQS8_c
VSS	53	197	DQS8_t
CB6, *NC*	54	198	VSS
VSS	55	199	CB7, *NC*
CB2, *NC*	56	200	VSS
VSS	57	201	CB3, *NC*
RESET_n	58	202	VSS
VDD	59	203	CKE1
CKE0	60	204	VDD
VDD	61	205	RFU
ACT_n	62	206	VDD
BG0	63	207	BG1
VDD	64	208	ALERT_n
A12/BC_n	65	209	VDD
A9	66	210	A11
VDD	67	211	A7
A8	68	212	VDD
A6	69	213	A5
VDD	70	214	A4
A3	71	215	VDD
A1	72	216	A2
VDD	73	217	VDD

Front Side Pin Label	Pin	Pin	Back side Pin Label
VSS	112	256	DQS5_t
DQ46	113	257	VSS
VSS	114	258	DQ47
DQ42	115	259	VSS
VSS	116	260	DQ43
DQ52	117	261	VSS
VSS	118	262	DQ53
DQ48	119	263	VSS
VSS	120	264	DQ49
TDQS15_t, DQS15_t, *DM6_n, DBI6_n, NC*	121	265	VSS
TDQS15_c, DQS15_c, *NC*	122	266	DQS6_c
VSS	123	267	DQS6_t
DQ54	124	268	VSS
VSS	125	269	DQ55
DQ50	126	270	VSS
VSS	127	271	DQ51
DQ60	128	272	VSS
VSS	129	273	DQ61
DQ56	130	274	VSS
VSS	131	275	DQ57
TDQS16_t, DQS16_t, *DM7_n, DBI7_n, NC*	132	276	VSS
TDQS16_c, DQS16_c, *NC*	133	277	DQS7_c
VSS	134	278	DQS7_t
DQ62	135	279	VSS
VSS	136	280	DQ63
DQ58	137	281	VSS
VSS	138	282	DQ59
SA0	139	283	VSS
SA1	140	284	VDDSPD
SCL	141	285	SDA
VPP	142	286	VPP
VPP	143	287	VPP
RFU	144	288	VPP

JEDEC Standard No. 21C (Aug. 2015), at Pages 4.20.27-10 to 4.20.27-11.

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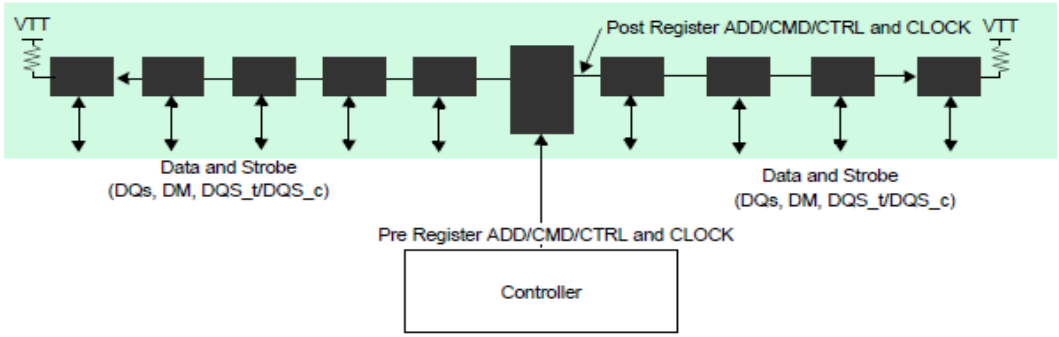
'912 Patent	Accused Instrumentalities
	Similarly, In Figure 4 of the DDR4 RDIMM specification, reproduced below, the JEDEC Standard No. 21C specification provides an example of RDIMM topologies illustrating the connection between the memory module and the memory controller of a computer system.  JEDEC Standard No. 21C (Dec. 2015), at Page 4.20.28-19. *See also* JEDEC Standard No. 21C (May 2019), at Page 4.20.28-19. In accordance with the JEDEC Standard No. 21C specification, the DDR4 RDIMM socket pin wiring assignment for connecting to a memory controller of a computer system is provided in Table 5, reproduced below.

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Table 5 — DDR4 288 Pin RDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label
12 V, NC	1	145	12 V, NC
VSS	2	146	VREFCA
DQ4	3	147	VSS
VSS	4	148	DQ5
DQ0	5	149	VSS
VSS	6	150	DQ1
TDQS9_t, DQS9_t, DM0n, DBI0_n, NC	7	151	VSS
TDQS9_c/QS9_c, NC	8	152	DQS0_c
VSS	9	153	DQS0_t
DQ6	10	154	VSS
VSS	11	155	DQ7
DQ2	12	156	VSS
VSS	13	157	DQ3
DQ12	14	158	VSS
VSS	15	159	DQ13
DQ8	16	160	VSS
VSS	17	161	DQ9
TDQS10_t, DQS10_t, DM1_n, DBI1_n, NC	18	162	VSS
TDQS10_c, DQS10_c, NC	19	163	DQS1_c
VSS	20	164	DQS1_t
DQ14	21	165	VSS
VSS	22	166	DQ15
DQ10	23	167	VSS
VSS	24	168	DQ11
DQ20	25	169	VSS
VSS	26	170	DQ21
DQ16	27	171	VSS
VSS	28	172	DQ17
TDQS11_t, DQS11_t, DM2_n, DBI2_n, NC	29	173	VSS
TDQS11_c, DQS11_c, NC	30	174	DQS2_c
VSS	31	175	DQS2_t
DQ22	32	176	VSS
VSS	33	177	DQ23
DQ18	34	178	VSS
VSS	35	179	DQ19
DQ28	36	180	VSS
VSS	37	181	DQ29
DQ24	38	182	VSS
VSS	39	183	DQ25

Front Side Pin Label	Pin	Pin	Back side Pin Label
CK0_t	74	218	CK1_t
CK0_c	75	219	CK1_c
VDD	76	220	VDD
VTT	77	221	VTT
KEY			
EVENT_n	78	222	PARITY
A0	79	223	VDD
VDD	80	224	BA1
BA0	81	225	A10/AP
RAS_n/A16	82	226	VDD
VDD	83	227	RFU
CS0_n	84	228	WE_n/A14
VDD	85	229	VDD
CAS_n/A15	86	230	NC, SAVE_n
ODT0	87	231	VDD
VDD	88	232	A13
CS1_n, NC	89	233	VDD
VDD	90	234	NC, A17
ODT1, NC	91	235	NC, C2
VDD	92	236	VDD
C0, CS2_n, NC	93	237	NC, CS3_n, C1
VSS	94	238	SA2
DQ36	95	239	VSS
VSS	96	240	DQ37
DQ32	97	241	VSS
VSS	98	242	DQ33
TDQS13_t, DQS13_t, DM4_n, DBI4_n, NC	99	243	VSS
TDQS13_c, DQS13_c, NC	100	244	DQS4_c
VSS	101	245	DQS4_t
DQ38	102	246	VSS
VSS	103	247	DQ39
DQ34	104	248	VSS
VSS	105	249	DQ35
DQ44	106	250	VSS
VSS	107	251	DQ45
DQ40	108	252	VSS
VSS	109	253	DQ41
TDQS14_t, DQS14_t, DM5_n, DBI5_n, NC	110	254	VSS

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'912 Patent	Accused Instrumentalities

Table 5 — DDR4 288 Pin RDIMM Pin Wiring Assignments

Front Side Pin Label	Pin	Pin	Back side Pin Label
TDQS12_t, DQS3_t, DM3_n, DBI3_n, NC	40	184	VSS
TDQS12_c, DQS12_c, NC	41	185	DQS3_c
VSS	42	186	DQS3_t
DQ30	43	187	VSS
VSS	44	188	DQ31
DQ26	45	189	VSS
VSS	46	190	DQ27
CB4, NC	47	191	VSS
VSS	48	192	CB5, NC
CB0, NC	49	193	VSS
VSS	50	194	CB1, NC
TDQS17_t, DQS17_t, DM8_n, DBI8_n, NC	51	195	VSS
TDQS17_c, DQS17_c, NC	52	196	DQS8_c
VSS	53	197	DQS8_t
CB6, NC	54	198	VSS
VSS	55	199	CB7, NC
CB2, NC	56	200	VSS
VSS	57	201	CB3, NC
RESET_n	58	202	VSS
VDD	59	203	CKE1, NC
CKE0	60	204	VDD
VDD	61	205	RFU
ACT_n	62	206	VDD
BG0	63	207	BG1
VDD	64	208	ALERT_n
A12/BC_n	65	209	VDD
A9	66	210	A11
VDD	67	211	A7
A8	68	212	VDD
A6	69	213	A5
VDD	70	214	A4
A3	71	215	VDD
A1	72	216	A2
VDD	73	217	VDD

Front Side Pin Label	Pin	Pin	Back side Pin Label
TDQS14_c, DQS14_c, NC	111	255	DQS5_c
VSS	112	256	DQS5_t
DQ46	113	257	VSS
VSS	114	258	DQ47
DQ42	115	259	VSS
VSS	116	260	DQ43
DQ52	117	261	VSS
VSS	118	262	DQ53
DQ48	119	263	VSS
VSS	120	264	DQ49
TDQS15_t, DQS15_t, DM6_n, DBI6_n, NC	121	265	VSS
TDQS15_c, DQS15_c, NC	122	266	DQS6_c
VSS	123	267	DQS6_t
DQ54	124	268	VSS
VSS	125	269	DQ55
DQ50	126	270	VSS
VSS	127	271	DQ51
DQ60	128	272	VSS
VSS	129	273	DQ61
DQ56	130	274	VSS
VSS	131	275	DQ57
TDQS16_t, DQS16_t, DM7_n, DBI7_n, NC	132	276	VSS
TDQS16_c, DQS16_c, NC	133	277	DQS7_c
VSS	134	278	DQS7_t
DQ62	135	279	VSS
VSS	136	280	DQ63
DQ58	137	281	VSS
VSS	138	282	DQ59
SA0	139	283	VSS
SA1	140	284	VDDSPD
SCL	141	285	SDA
VPP	142	286	VPP
VPP	143	287	VPP
RFU	144	288	VPP

See JEDEC Standard No. 21C (Dec. 2015), at Pages 4.20.28-10 to 4.20.28-11. *See also* JEDEC Standard No. 21C (May 2019), at Pages 4.20.28-10 to 4.20.28-11.

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'912 Patent	**Accused Instrumentalities**
	JESD 248A (Mar. 2018), at Pages 7-9; *see also*, *supra*, [16pre].
[16.1] a printed circuit board;	For example, the JEDEC Standard No. 21C specification describes component types and placements as follows: "5.1 Component Types and Placement Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for DDR4 SDRAM signals." JEDEC Standard No. 21C (Aug. 2015), at Page 4.20.27-16; JEDEC Standard No. 21C (Dec. 2015), at Page 4.20.28-17; JEDEC Standard No. 21C (May 2019), at Page 4.20.28.18; JESD 248A (Mar. 2018), at Page 18. The JEDEC Standard No. 21C specification further provides "[p]referred rules" DIMM routing space constraints in relation to printed circuit board design. These rules includes via size, pad spacing, line spacing, and the like. *See* JEDEC Standard No. 21C (Aug. 2015), at Pages 4.20.27-26 to 4.20.27-27; JEDEC Standard No. 21C (Dec. 2015), at Page 4.20.28-28; JEDEC Standard No. 21C (May 2019), at Page 4.20.28-31; JESD 248A (Mar. 2018), at Page 31.
[16.2] a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;	On information and belief, the Disputed Memory Modules include a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks. In Figure 10, reproduced below, the JEDEC Standard No. 21C specification provides an example of a plurality of DDR4 memory devices coupled to the printed circuit board, with the DDR4 memory devices arranged in a first number of ranks.

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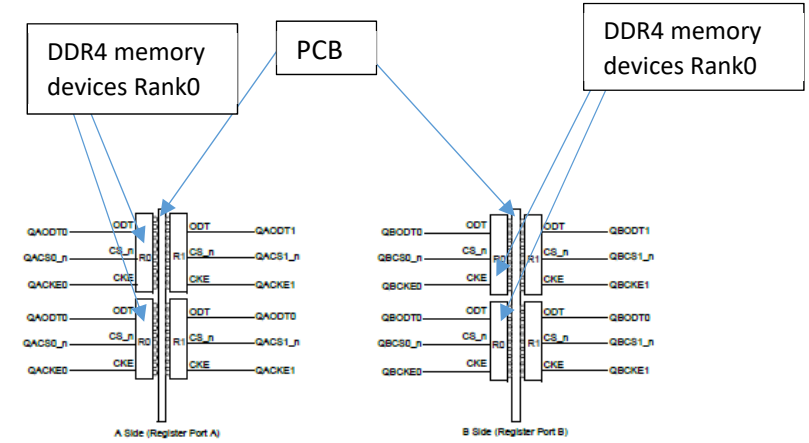
'912 Patent	Accused Instrumentalities
	 **Figure 10 — DDR4 2R/4R/8R/16R (planar/3DS) Control Wiring** JEDEC Standard No. 21C (Aug. 2015), at Page 4.20.27-29; JEDEC Standard No. 21C (Dec. 2015) (Figure 13), at Page 4.20.28-31; JEDEC Standard No. 21C (May 2019) (Figure 13), at Page 4.20.28-34; JESD 248A (Mar. 2018), at Page 35 (Figure 15). As noted in Figure 10, the plurality of DDR memory devices may be arranged in two ("2R"), four ("4R"), eight ("8R"), or sixteen ("16R") ranks. The plurality of DDR memory devices coupled to the printed circuit board may be monolithic (*i.e.*, single-die) DRAM. Alternatively, the plurality of DDR memory devices may be multi-die DRAM packages such as dual-die package ("DDP," featuring two dies per package), or stacked 3DS (featuring two, four, or eight dies per package).

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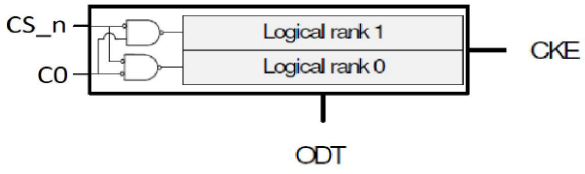
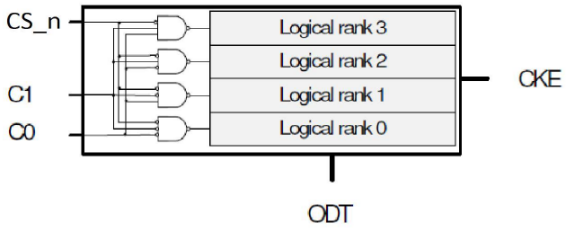
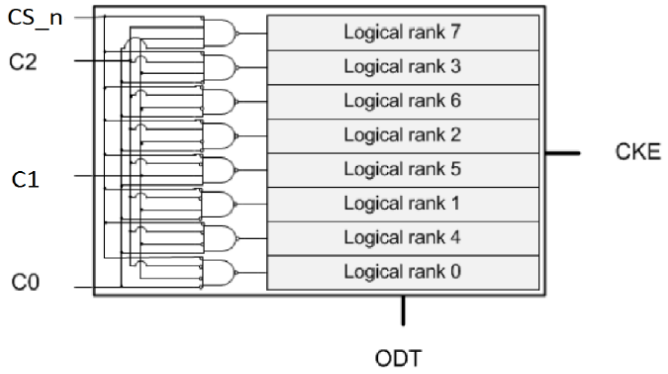
'912 Patent	**Accused Instrumentalities**
	See, e.g., Add. No. 1 to JESD 79-4, 3D Stacked DRAM, JESD 79-4-1-B, at 5-7 (Feb. 2021) (illustration of 2H, 4H, and 8H 3DS DRAM packages):  Figure 3 — 2-1-1-1 Device (2H)  Figure 4 — 4-1-1-1 Device (4H)  Figure 5 — 8-1-1-1 Device (8H)
[16.3] a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,	The JESD 82-31A standard "defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the DDR4 Registering Clock Driver (RCD) with parity for driving address and control nets on DDR4 RDIMM and LRDIMM applications." JESD 82-31A (Aug. 2019), at Page 1. The DDR4 RCD comprises a logic element and a register. Figure 28 from JESD 82-31A, reproduced below, identifies the logic element and the register.

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	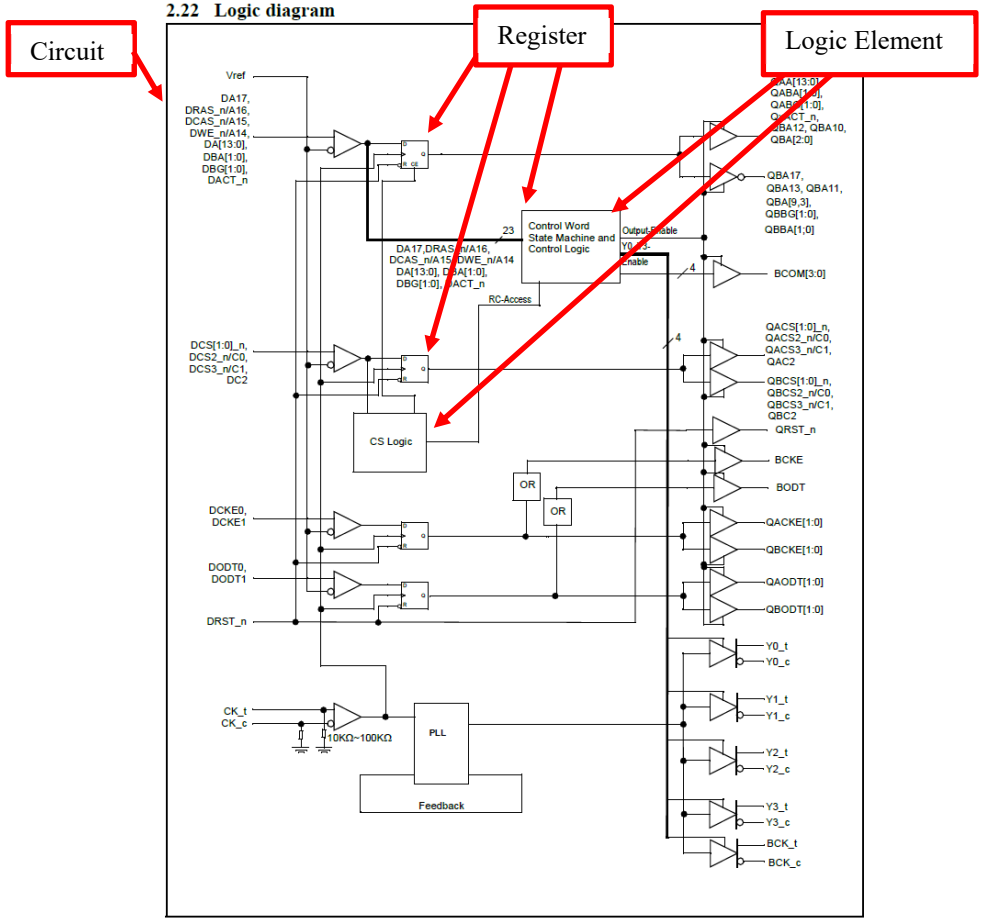 Figure 28 — Logic diagram (positive logic) JESD 82-31A (Aug. 2019), at Page 66.

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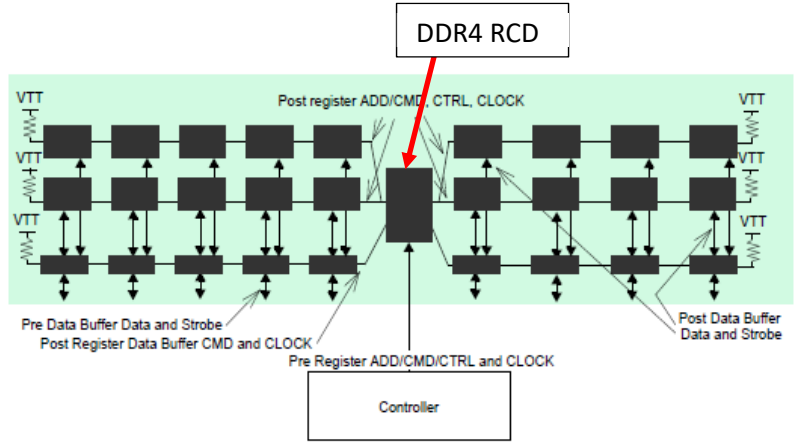
'912 Patent	Accused Instrumentalities
	In Figure 3 of the DDR4 LRDIMM specification, reproduced below, the JEDEC Standard No. 21C specification provides an example of a LRDIMM configuration where the DDR4 RCD is coupled to the printed circuit board.  **Figure 3 — LRDIMM Topologies** JEDEC Standard No. 21C (Aug. 2015), at Page 4.20.27-17.

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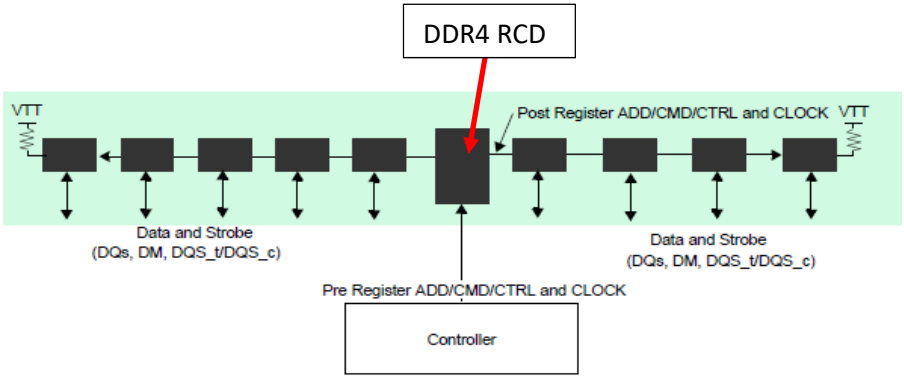
'912 Patent	**Accused Instrumentalities**
	Similarly, in Figure 4 of the DDR4 RDIMM specification, reproduced below, the JEDEC Standard No. 21C specification provides an example of a RDIMM configuration where the DDR4 RCD is coupled to the printed circuit board.  JEDEC Standard No. 21C (Dec. 2015), at Page 4.20.28-19. *See also* JEDEC Standard No. 21C (May 2019), at Page 4.20.28-19.
[16.4] the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,	JESD 82-31A also demonstrates that the logic element (DDR4 RCD) receives a set of input signals from the computer system, as described in the Terminal functions table, Table 21. As shown below, the set of input signals comprises: at least one row/column address signal (any one or more of DA13:0, DWES_n/A14, DCAS_n/A15, DRAS_n/A16, DA17); bank address signals (any two signals of the bank address signals, DBA1:0, or bank group address signals, DBG1:0); and at least one chip-select signal (any one chip select of the two input chip select signals: DCS1:0).

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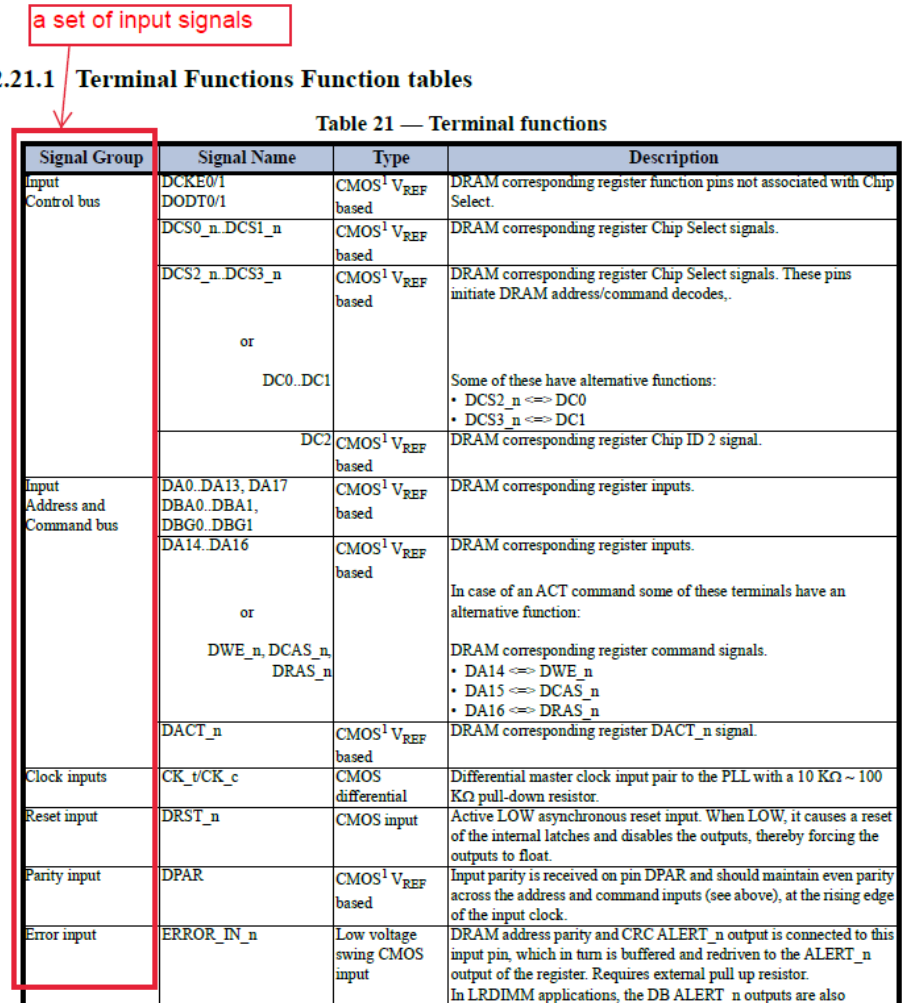
'912 Patent	Accused Instrumentalities
	

2.21.1 Terminal Functions Function tables

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] V_{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes,. Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC2	CMOS[1] V_{REF} based	DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] V_{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS[1] V_{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS[1] V_{REF} based	DRAM corresponding register DACT_n signal.
Clock inputs	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10 KΩ ~ 100 KΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS[1] V_{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also

JESD 82-31A (Aug. 2019), at Page 61.

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'912 Patent	Accused Instrumentalities
	Figure 28, reproduced below, also demonstrates that the logic element (DDR4 RCD) receives a set of input signals from the computer system.

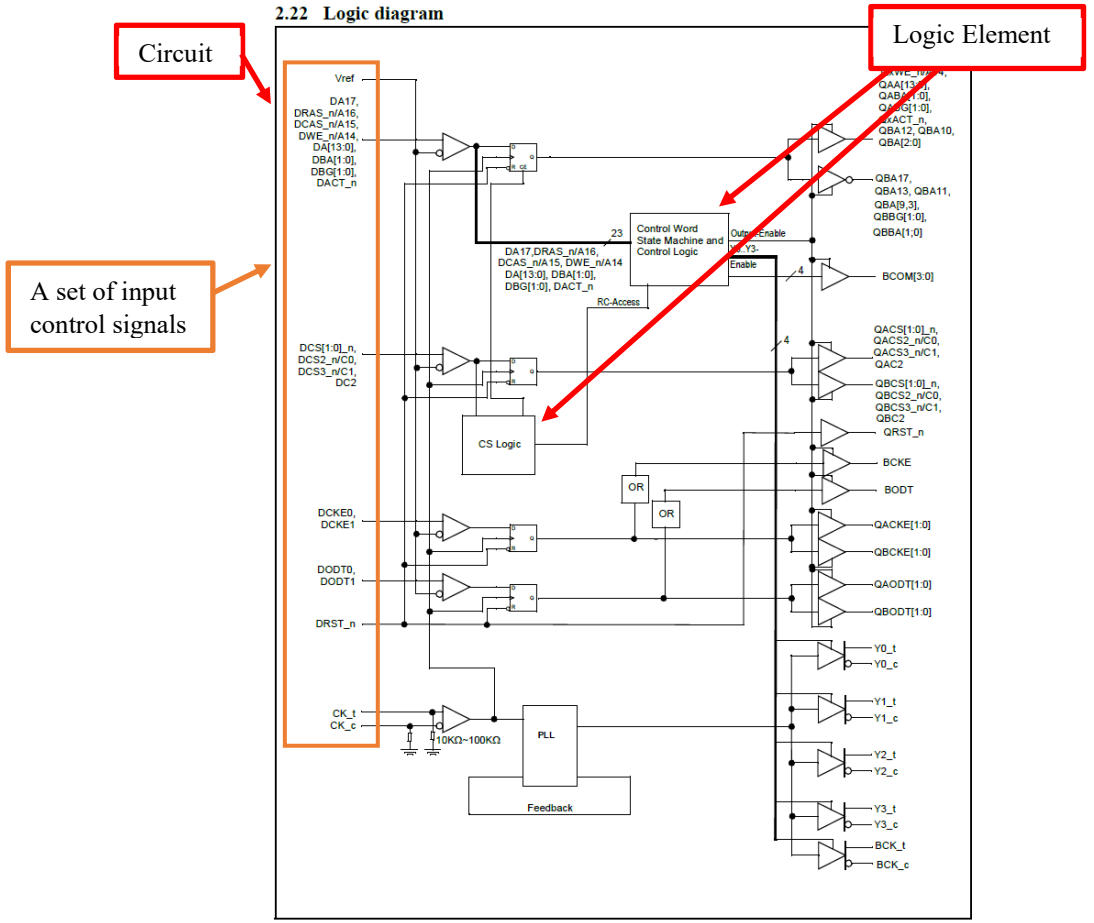

Figure 28 — Logic diagram (positive logic)

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'912 Patent	Accused Instrumentalities
	JESD 82-31A (Aug. 2019), at Page 66.
[16.5] the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,	The set of input signals to the DDR4 RCD includes two input CS and other control and address signals that can control two ranks (second number of ranks) of eighteen 8-bit DDR memory devices (second number of memory devices). For example, DDR4 SDRAM devices arranged in a first rank are controlled using a first input chip select signal (DCS0) along with control and address signals, while other DDR4 SDRAM devices arranged in a second rank are controlled using a second input chip select signal (DCS1) along with control and address signals. JESD 82-31A provides that in normal operating modes, such as the Direct DualCS or Direct QuadCS modes, each input chip select signal, which is used to control one rank, is received by the register that in turn outputs a chip select signal to control one rank of DDR memory devices. *See* JESD 82-31A (Aug. 2019), at Page 2 ("In Direct DualCS mode (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. . . . In Direct QuadCS mode (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n."). In Encoded QuadCS mode, the DDR4 RCD specification provides for the generation of four chip select signals, one for each rank of a quad rank DDR4 RDIMM or LRDIMM by decoding the two input chip select signals using another input signal, namely DC0, as the encoding input. *See* JESD 82-31A (Aug. 2019), at Page 2 ("In Encoded QuadCS mode (DA[1:0] = 11), two copies of four output chip selects, i.e. QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input."). These modes are summarized in Table 1, reproduced below.

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'912 Patent	Accused Instrumentalities
	Table 1 — Generic DCS - QxCS Mapping **Input CS** / **Output CS**: Direct DualCS mode; Direct QuadCS mode; Encoded QuadCS mode DCS0_n: QxCS0_n; QxCS0_n; QxCS0_n, QxCS1_n DCS1_n: QxCS1_n; QxCS1_n; QxCS2_n, QxCS3_n DCS2_n/DC0: n/a; QxCS2_n; n/a DCS3_n/DC1: n/a; QxCS3_n; n/a JESD 82-31A (Aug. 2019), at Page 3. JESD 82-31A thus demonstrates that in Encoded Quad CS Mode, the set of input signals is configured to control a second number of DDR memory devices (18) smaller than the first number of DDR memory devices (36), and the second number of ranks (2) less than the first number of ranks (4). Memory modules featuring DDP DRAM are configured to operate in substantially the same way in material aspects as those featuring monolithic (*i.e.*, single-die) DRAM. For example, JESD 82-31A provides that one of the two ways to provide the required four chip-select signals is through the Encoded QuadCS Mode: **2.2.2 Quad CS Modes** For DIMMs using dual-die packages there is a need for four CS signals rather than the standard two. For these modules two modes are available where four CS outputs are available. The memory controller can select by programming the CS mode control bits which of the two modes it wants to utilize. There are two ways of accomplishing this: • by using four CS inputs from the host (DCS[3:0]_n). This is the Direct QuadCS mode. See Chapter 2.2.1, "Direct CS Modes," above. • by using two CS inputs and one of the chip ID inputs from the host (DCS[1:0]_n and DC0). See Chapter 2.2.3, "Encoded QuadCS Mode," below.

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'912 Patent	Accused Instrumentalities
	Id. at 3. Similarly, the JESD 79-4-1B standard further provides that DIMMs featuring ranks of 3DS DRAM operate in substantially the same way in material aspects to DIMMs featuring monolithic (*i.e.*, single-die) DRAM. For example, JESD 79-4-1B provides that the required signals to select a rank on the module are generated in in a manner similar to the "Encoded QuadCS mode" by using a combination of chip-select (CS) and chip-ID signals: **2.5 Logical Rank Addressing** The 3DS package is organized into two, four or eight logical ranks. For DDR4 3DS devices, the logical ranks are selected by the Chip ID bus C[2:0]. The functional behavior of logical rank(s) should not deviate from monolithic DDR4 SDRAMs (specified in JESD79-4A), except when noted in this document. Each logical rank may be implemented as a single slice but the DDR4 3DS addendum doesn't require this to be the case. **2.6 3D Stack Organizations** Table 1, "Supported 3D Stack Organizations," indicates valid configurations supported by the DDR4 3DS addendum. **Table 1 — Supported 3D Stack Organizations** | Logical Ranks | # of CS_n | Chip ID | # of CKE | # of ODT | |---|---|---|---|---| | 2 | 1 | C0 | 1 | 1 | | 4 | 1 | C0, C1 | 1 | 1 | | 8 | 1 | C0, C1, C2 | 1 | 1 | JESD 79-4-1B at 4.

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See also, e.g., *id.* at 5-8:

Table 2 — DDR4 Address Table: 2H Stacked SDRAM

DDR4 3DS Address Table: 2H 3D Stacked SDRAM									
3DS Logical Rank Organization						3DS Package Organization			
Density	x4 Page Size	x8 Page Size	MSB Address			Capacity	Logical Rank	CS_n	C0
			Col	Row					
				x4 Die	x8 Die				
4 Gb	512 B	1 KB	A9	A15	A14	8 Gb	0	L	L
							1	L	H
8 Gb	512 B	1 KB	A9	A16	A15	16 Gb	0	L	L
							1	L	H
16 Gb	512 B	1 KB	A9	A17	A16	32 Gb	0	L	L
							1	L	H

Table 3 — DDR4 Address Table: 4H Stacked SDRAM

DDR4 3DS Address Table: 4H 3D Stacked SDRAM										
3DS Logical Rank Organization						3DS Package Organization				
Density	x4 Page Size	x8 Page Size	MSB Address			Capacity	Logical Rank	CS_n	C1	C0
			Col	Row						
				x4 Die	x8 Die					
4 Gb	512 B	1 KB	A9	A15	A14	16 Gb	0	L	L	L
							1	L	L	H
							2	L	H	L
							3	L	H	H
8 Gb	512 B	1 KB	A9	A16	A15	32 Gb	0	L	L	L
							1	L	L	H
							2	L	H	L
							3	L	H	H
16 Gb	512 B	1 KB	A9	A17	A16	64 Gb	0	L	L	L
							1	L	L	H
							2	L	H	L
							3	L	H	H

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Table 4 — DDR4 Address Table: 8H Stacked SDRAM

DDR4 3DS Address Table: 8H 3D Stacked SDRAM											
3DS Logical Rank Organization						3DS Package Organization					
Density	x4 Page Size	x8 Page Size	MSB Address			Capacity	Logical Rank	CS_n	C2	C1	C0
			Col	Row							
				x4 Die	x8 Die						
4 Gb	512 B	1 KB	A9	A15	A14	32 Gb	0	L	L	L	L
							1	L	L	L	H
							2	L	L	H	L
							3	L	L	H	H
							4	L	H	L	L
							5	L	H	L	H
							6	L	H	H	L
							7	L	H	H	H
8 Gb	512 B	1 KB	A9	A16	A15	64 Gb	0	L	L	L	L
							1	L	L	L	H
							2	L	L	H	L
							3	L	L	H	H
							4	L	H	L	L
							5	L	H	L	H
							6	L	H	H	L
							7	L	H	H	H
16 Gb	512 B	1 KB	A9	A17	A16	128 Gb	0	L	L	L	L
							1	L	L	L	H
							2	L	L	H	L
							3	L	L	H	H
							4	L	H	L	L
							5	L	H	L	H
							6	L	H	H	L
							7	L	H	H	H

NOTE These diagrams show only the logical organizations of these devices. No 1:1 relationship to physical organizations is implied. The Logical Rank 0 is considered the "primary die", regardless of its physical arrangement.

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[16.6] the circuit generating a set of output signals in response to the set of input signals,	JESD 82-31A also demonstrates that the circuit (DDR4 RCD) generates a set of output signals in response to the set of input signals, as described in the Terminal functions table, Table 21. As shown below, the set of output signals includes any of the register output address signals Q[A:B]A[13:0] corresponding to the set of input signals; any of the register output bank address or bank group address signal Q[A:B]BA[1:0] or Q[A:B]BG[1:0] corresponding to the set of input signals; and the register output chip select signals corresponding to the Encoded QuadCS mode.

a set of output signals

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS[2]	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n	CMOS[2]	Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS[2]	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS[2]	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.

JESD 82-31A (Aug. 2019), at Page 62.

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Figure 28, reproduced below, also demonstrates that the circuit (DDR4 RCD) generates a set of output signals in response to the set of input signals.

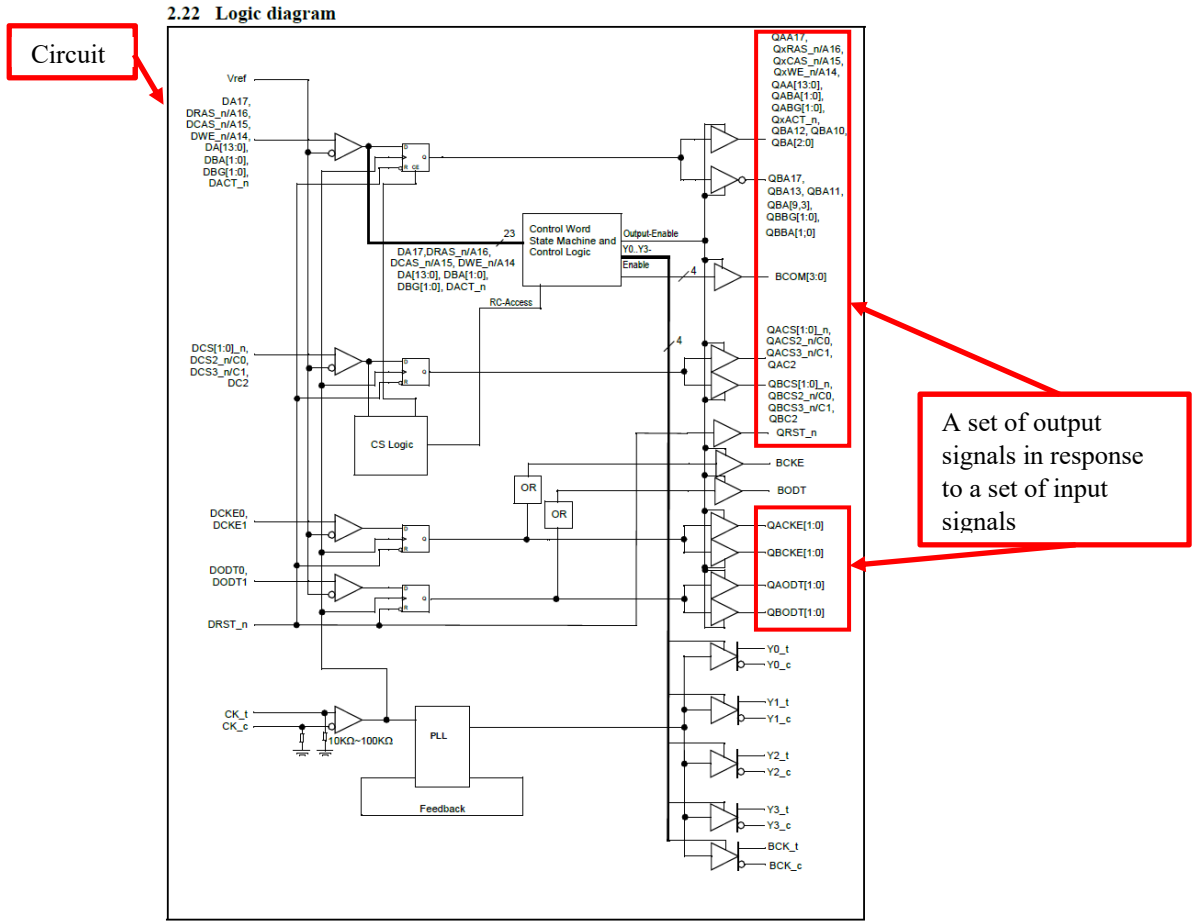

Figure 28 — Logic diagram (positive logic)

JESD 82-31A (Aug. 2019), at Page 66.

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'912 Patent	**Accused Instrumentalities**
[16.7] the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,	JESD 82-31A also demonstrates that in Encoded Quad CS Mode, the set of output signals is configured to control the first number of DDR memory devices (36) arranged in the first number of ranks (4). As demonstrated in Table 2, reproduced below, in Encoded Quad CS Mode, the set of output signals includes four output chip select signals, two copies each, namely Q[A:B]CS[3:0]. The set of output signals is configured to control the first number of DDR memory devices (36) arranged in the first number of ranks (4). *See also* JESD 82-31A (Aug. 2019) at 3. ("When F0RC0D DA[1:0] = 11 the DDR4 register decodes two sets of four QxCS_n outputs from two DCS_n inputs by using the DC0 as the encoding input.").

Table 2 — DCS, DC - QxCS, QxC Mapping in Encoded QuadCS mode

DCS1_n	DCS0_n	DC0	DC2	QxCS[3:0]_n	QxC2
H	H	X	0	HHHH	No change
		X	1		
H	L	0	0	HHHL	0
		0	1		1
		1	0	HHLH	0
		1	1		1
L	H	0	0	HLHH	0
		0	1		1
		1	0	LHHH	0
		1	1		1
L	L	0	0	HLHL[1]	0
		0	1		1
		1	0	LHLH[1]	0
		1	1		1

1.Only one DCSx_n input can be asserted for DRAM MRS and DRAM read commands

JESD 82-31A (Aug. 2019), at Page 3.

See also, supra, analysis for Element 16.5.

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'912 Patent	**Accused Instrumentalities**
[16.8] wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and	The DDR4 SDRAM specification JESD 79-4C "allows programmability of a given device on a rank" through the "per DRAM addressability" ("PDA") feature. 4.14 Per DRAM Addressability DDR4 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank. 1. Before entering 'per DRAM addressability (PDA)' mode, the write leveling is required. 2. Before entering 'per DRAM addressability (PDA)' mode, the following Mode Register setting is possible. -RTT_PARK MR5 {A8:A6} = Enable -RTT_NOM MR1 {A10:A9:A8} = Enable 3. Enable 'per DRAM addressability (PDA)' mode using MR3 bit "A4=1". 4. In the 'per DRAM addressability' mode, all MRS command is qualified with DQ0 for x4 and x8, and DQL0 for x16. DRAM captures DQ0 for x4 and x8, and DQL0 for x16 by using DQS_c and DQS_t for x4 and x8, DQSL_c and DQSL_t for x16 signals as shown Figure 36 . If the value on DQ0 for x4 and x8, and DQL0 for x16 is 0 then the DRAM executes the MRS command. If the value on DQ0 is 1, then the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits. JESD 79-4C (January 2020), at Page 63. In PDA mode, PDA commands include Mode Register Set (MRS) with DQ0=Low of the target DDR memory device to be programmed, as shown in the Simplified State Diagram of Figure 6, reproduced below.

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'912 Patent	Accused Instrumentalities

JEDEC Standard No. 79-4C
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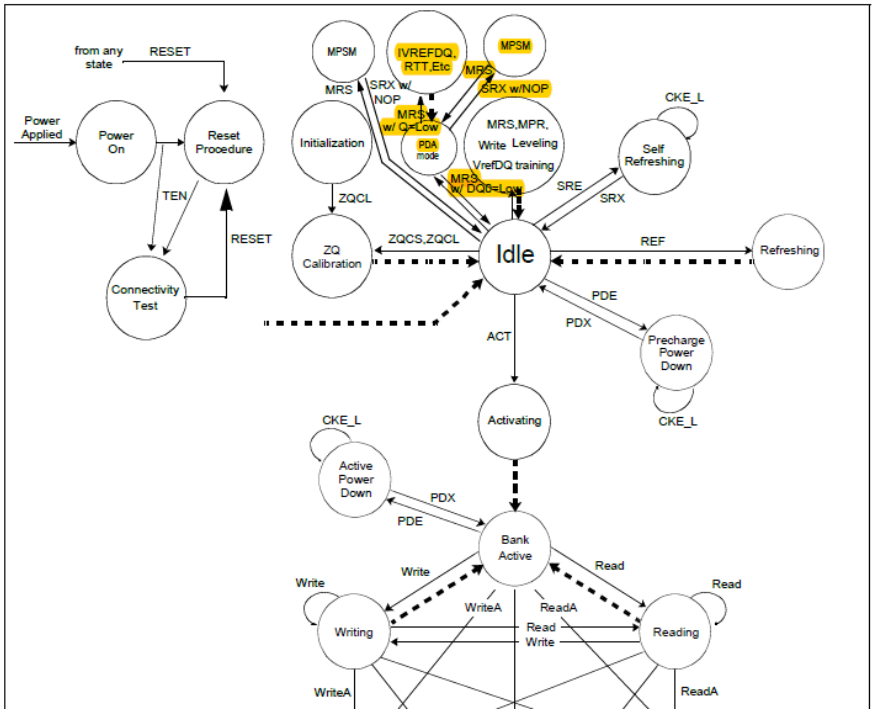
3 Functional Description

3.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than on bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.



JESD 79-4C (January 2020), at Page 10.

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'912 Patent	Accused Instrumentalities
	As set forth in JESD 79-4C Table 35, reproduced in relevant part below, the MRS function includes at least one address signal, bank address signals, and a chip-select signal.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 35 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12

JESD 79-4C (January 2020), at Page 29. MR3 is a MRS command that includes one row address signal A4=1 that sets the operating mode to the PDA Mode, as defined in Table 22, reproduced below.

MR3

Table 22 — Mode Register 3

Address	Operating Mode	Description	
BG1	RFU	0 = must be programmed to 0 during MRS	
BG0, BA1:BA0	MR Select	000 = MR0	100 = MR4
		001 = MR1	101 = MR5
		010 = MR2	110 = MR6
		011 = MR3	111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS	
A13	RFU	0 = must be programmed to 0 during MRS	
A12:A11	MPR Read Format	00 = Serial	10 = Staggered
		01 = Parallel	11 = Reserved
A10:A9	Write CMD Latency when CRC and DM are enabled	(see Table 24)	
A8:A6	Fine Granularity Refresh Mode	(see Table 23)	
A5	Temperature sensor readout	0 : disabled	1: enabled
A4	Per DRAM Addressability	0 = Disable	1 = Enable
A3	Geardown Mode	0 = 1/2 Rate	1 = 1/4 Rate

JESD 79-4C (January 2020), at Page 22.

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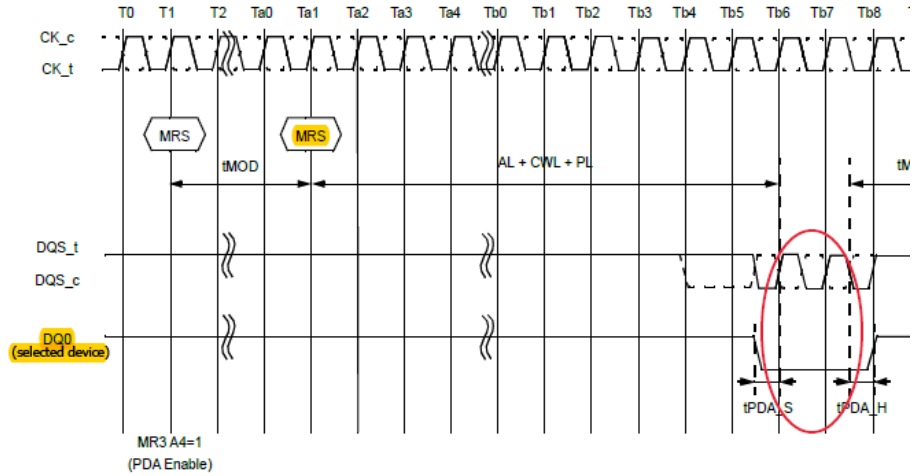
	As illustrated above, JESD 79-4C provides that the set of output signals includes a chip select signal corresponding to the encoded input chip select signal associated with MR3 which selects one of the first number of ranks, and with DQ0=Low selects one selected DDR memory device of the selected rank. Only the selected DDR memory device performs the PDA command. Figure 38, reproduced below, is a timing diagram illustrating a selected device of a rank of DDR memory device executing a PDA command when its DQ0 is sampled Low.  **Figure 38 — PDA using Burst Chop 4** JESD 79-4C (January 2020), at Page 65. In the context of DDR4 LRDIMM, the JEDEC Standard No. 21C provides that the circuit further responds to a command signal and the set of input signals from the computer system by generating BCOM write command over BCOM[3:0] to control the DDR4 LRDIMM data buffers in order to forward the computer system data (DQ) signals to the DRAMs which use their DQ0 for device selection. *See* JESD82-31A (Aug. 2019), at Page 19 ("For MRS Write commands in PDA (Per DRAM Addressability) mode when the DIMM type bit in F0RC0D is set to '0' (LRDIMM), the

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	DDR4RCD02 generates a BCOM Write command instead of a BCOM MRS Write command in order to forward the data buffer's host interface DQ inputs to the DRAMs which use their DQ0 pins for device selection."). *See also*, JESD82-31A (Aug. 2019), at Page 16:

Table 7 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

This claim element is literally infringed (directly and/or indirectly) by Samsung, as described herein, but is also infringed under the doctrine of equivalents because the structure and functionality provided by Samsung is being used to satisfy this claim limitation and therefore there is no vitiation of this element, and the Accused Instrumentalities incorporate structure and functionality that is not substantially different from the requirements of this limitation because they achieve substantially or exactly the same function, in substantially or exactly the same way as set forth in the claim element (as described herein), and achieve substantially or exactly the same result.

Accused Instrumentalities that are compliant with the DDR4 standard are configured to transmit command signals to at least one DDR memory device. To the extent that the Accused Instrumentalities do not literally meet this claim limitation, they perform this functionality in

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'912 Patent	Accused Instrumentalities
	substantially the same way by conveying, through one or more electrical connections, command signals to DDR memory devices, which command signals include MRS commands and DQ0 values. The Accused Instrumentalities achieve the substantially same result in that DDR memory devices are provided with command signals (including MRS commands (MR3) and DQ0 values) over the one or more electrical connections. Therefore, to the extent the Accused Instrumentalities do not literally meet the claim element, there is an insubstantial difference in how the Accused Instrumentalities operate compared to this element, and the Accused Instrumentalities at least equivalently meet this limitation.
[16.9] a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.	In Figure 28, reproduced below, JESD82-31A indicates that the DDR4 RCD includes a PLL that is operatively coupled to the plurality of DDR memory devices (via the complementary clock outputs to DDR4 SDRAM devices Y3:0_t, Y3:0_c), the logic element (via connections to at least multiple logic blocks within the logic element), and the register (via connections to many registers within the register, e.g. state machine, control words registers CW Table, CW state machine).

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	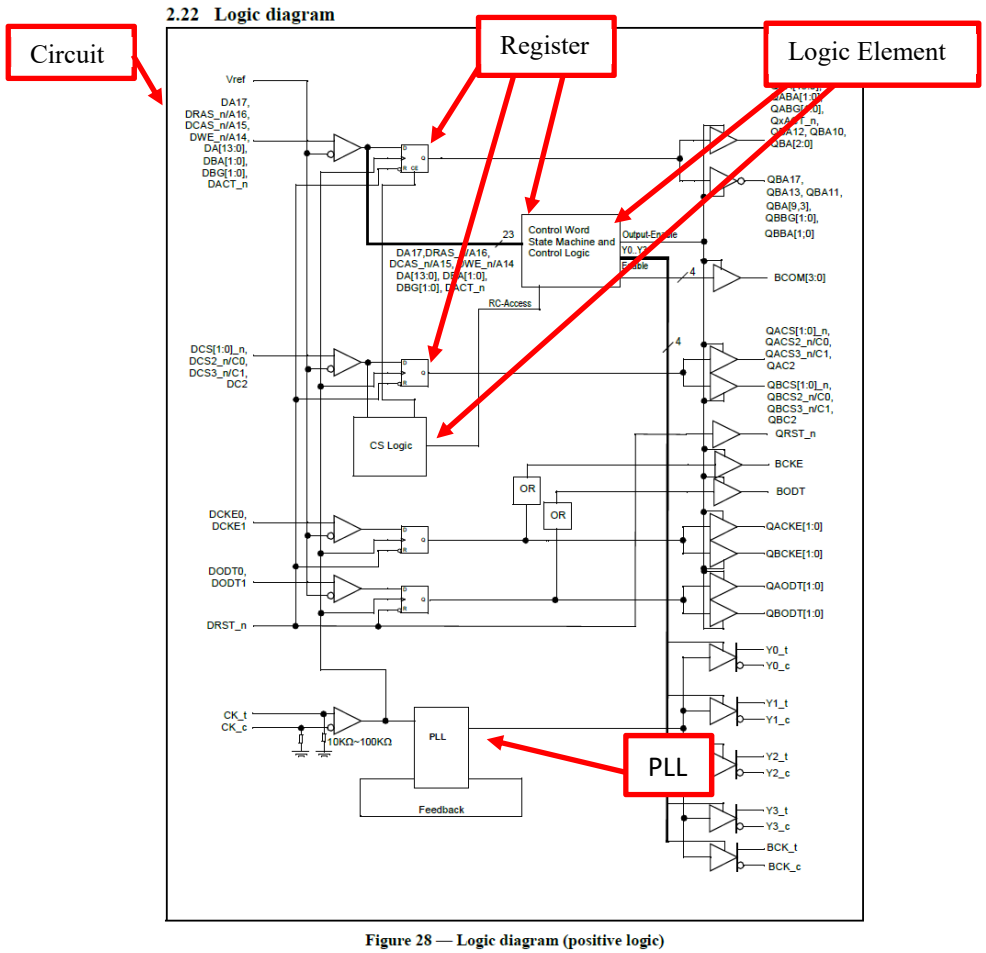 Figure 28 — Logic diagram (positive logic) JESD 82-31A (Aug. 2019), at Page 66.

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'912 Patent	**Accused Instrumentalities**
[16.10] wherein the command signal is transmitted to only one DDR memory device at a time.	As illustrated above, JESD 79-4C provides the PDA feature for transmitting the command signal to only one DDR memory device at a time: 4.14 Per DRAM Addressability DDR4 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank. 1. Before entering 'per DRAM addressability (PDA)' mode, the write leveling is required. 2. Before entering 'per DRAM addressability (PDA)' mode, the following Mode Register setting is possible. -RTT_PARK MR5 {A8:A6} = Enable -RTT_NOM MR1 {A10:A9:A8} = Enable 3. Enable 'per DRAM addressability (PDA)' mode using MR3 bit "A4=1". 4. In the 'per DRAM addressability' mode, all MRS command is qualified with DQ0 for x4 and x8, and DQL0 for x16. DRAM captures DQ0 for x4 and x8, and DQL0 for x16 by using DQS_c and DQS_t for x4 and x8, DQSL_c and DQSL_t for x16 signals as shown Figure 36 . If the value on DQ0 for x4 and x8, and DQL0 for x16 is 0 then the DRAM executes the MRS command. If the value on DQ0 is 1, then the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits. JESD 79-4C (January 2020), at Page 63. In PDA mode, PDA commands include Mode Register Set (MRS) with DQ0=Low of the target DDR memory device to be programmed, as shown in the Simplified State Diagram of Figure 6, reproduced below.

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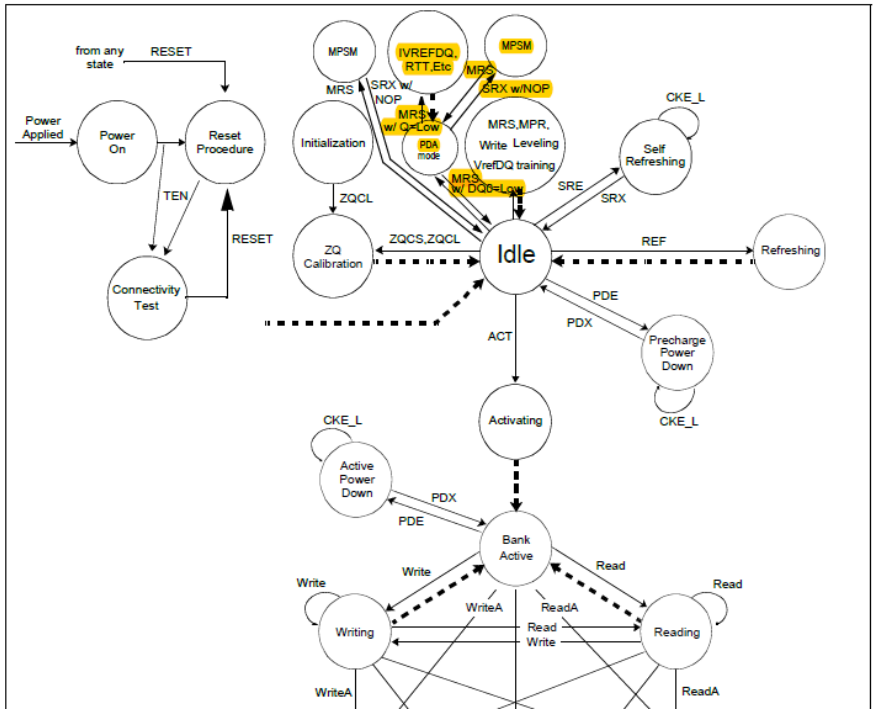
3 Functional Description

3.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than on bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.



JESD 79-4C (January 2020), at Page 10.

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Exhibit 5

'912 Patent	Accused Instrumentalities
	As set forth in JESD 79-4C Table 35, reproduced in relevant part below, the MRS function includes at least one address signal, bank address signals, and a chip-select signal.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 35 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V		OP Code			12

JESD 79-4C (January 2020), at Page 29. MR3 is a MRS command that includes one row address signal A4=1 that sets the operating mode to the PDA Mode, as defined in Table 22, reproduced below.

MR3

Table 22 — Mode Register 3

Address	Operating Mode	Description	
BG1	RFU	0 = must be programmed to 0 during MRS	
BG0, BA1:BA0	MR Select	000 = MR0	100 = MR4
		001 = MR1	101 = MR5
		010 = MR2	110 = MR6
		011 = MR3	111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS	
A13	RFU	0 = must be programmed to 0 during MRS	
A12:A11	MPR Read Format	00 = Serial	10 = Staggered
		01 = Parallel	11 = Reserved
A10:A9	Write CMD Latency when CRC and DM are enabled	(see Table 24)	
A8:A6	Fine Granularity Refresh Mode	(see Table 23)	
A5	Temperature sensor readout	0 : disabled	1: enabled
A4	Per DRAM Addressability	0 = Disable	1 = Enable
A3	Geardown Mode	0 = 1/2 Rate	1 = 1/4 Rate

JESD 79-4C (January 2020), at Page 22.

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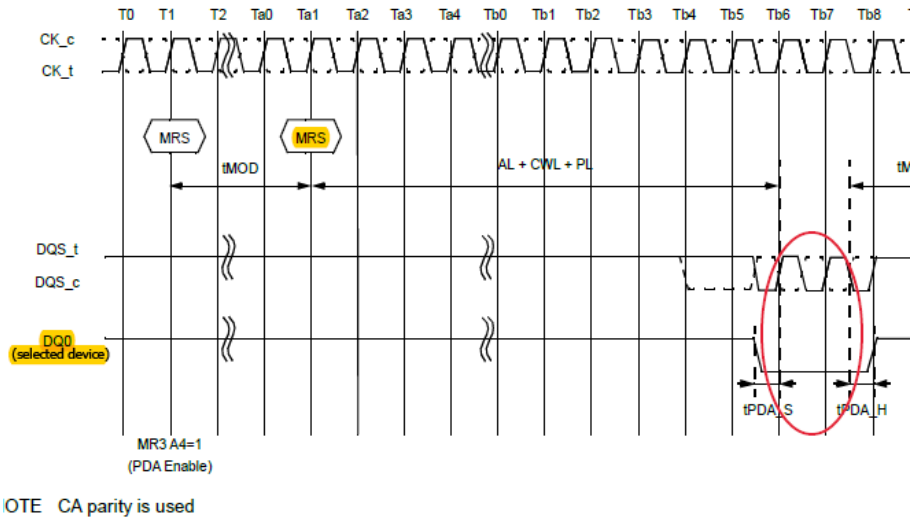
	This is further illustrated in JESD 79-4C, Figure 38:  **Figure 38 — PDA using Burst Chop 4** JESD 79-4C (January 2020), at Page 65. In the context of to DDR4 LRDIMM, the JEDEC Standard No. 21C provides that the circuit further responds to a command signal and the set of input signals from the computer system by generating BCOM write command over BCOM[3:0] to control the DDR4 LRDIMM data buffers in order to forward the computer system data (DQ) signals to the DRAMs which use their DQ0 for device

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'912 Patent	Accused Instrumentalities
	selection. *See also* JESD82-31A (Aug. 2019), at Page 19 ("For MRS Write commands in PDA (Per DRAM Addressability) mode when the DIMM type bit in F0RC0D is set to '0' (LRDIMM), the DDR4RCD02 generates a BCOM Write command instead of a BCOM MRS Write command in order to forward the data buffer's host interface DQ inputs to the DRAMs which use their DQ0 pins for device selection."). *See also*, JESD82-31A (Aug. 2019), at Page 16:

Table 7 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

This claim element is literally infringed (directly and/or indirectly) by Samsung, as described herein, but is also infringed under the doctrine of equivalents because the structure and functionality provided by Samsung is being used to satisfy this claim limitation and therefore there is no vitiation of this element, and the Accused Instrumentalities incorporate structure and functionality that is not substantially different from the requirements of this limitation because they achieve substantially or exactly the same function, in substantially or exactly the same way as set forth in the claim element (as described herein), and achieve substantially or exactly the same result.

Accused Instrumentalities that are compliant with the DDR4 standard are configured to transmit command signals to only one DDR memory device at a time. To the extent that the Accused Instrumentalities do not literally meet this claim limitation, they perform this functionality in

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	substantially the same way by conveying an MRS command (MR3) and a DQ0 value to a DDR memory device while in PDA mode. Specifically, only one DDR memory device that receives the MRS command (MR3) and DQ0=Low will perform the command when PDA mode is enabled, while DDR memory devices that receive the MRS command (MR3) but do not receive DQ0=Low will not perform the command. The Accused Instrumentalities achieve the substantially same result by sending an MRS command (MR3) to DDR memory devices in which only one DDR memory device is provided with DQ0=Low. Since only one of the DDR memory devices receives DQ0=Low, only that DDR memory device will perform the MRS command (MR3). Therefore, to the extent the Accused Instrumentalities do not literally meet the claim element, there is an insubstantial difference in how the Accused Instrumentalities operate compared to this element, and the Accused Instrumentalities at least equivalently meet this limitation.